Back Illuminated Vertically Pinned Photodiode with in Depth Charge Storage

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***Abstract*—A novel 1.4µm pitch pixel architecture dedicated for backside process with embedded vertically pinned photodiode is investigated. The proof of a vertical pinning is made thanks to a study of the maximum diode depletion potential for different diode widths. Diode doping strategy is described in order to optimize in-depth charge storage. Simulation results show good matching when compared to scanning capacitance microscopy (SCM). A new silicon on insulator (SOI) wafer with embedded ONO broadband antireflective coating (ARC) fabrication technique is presented and demonstrates further improvement in terms of quantum efficiency (QE), with 63% in green spectrum. Process solutions such as additional thermal treatment are provided to control maximum diode depletion potential. A transfer gate (TG) is stacked above the photodiode and its according charge transfer technique is investigated. Pixel performances show full-well capacity of more than 11000 electrons.**

***Index Terms*—Active pixel sensor, CMOS image sensor, backside illumination, full-well capacity, in depth charge storage, vertically pinned photodiode.**

I. INTRODUCTION

MOST of today's CMOS image sensors (CIS) use a so-called pinned photodiode. Thanks to diode full depletion and correlated double sampling these pixels offer the best noise performances at low light levels [1]. Due to continuous CIS pixel size shrinking [2-3], full-well capacity is dramatically reduced. As the signal-to-noise ratio is limited by photon shot noise at high light level [4], we have to recover pixel charge capability to save this figure.

In most pixel architectures, photodiodes remain planar i.e. the photodiode pinning layers are parallel to the silicon surface and the photo-generated charges are stored in the vicinity of silicon surface. Recently, the idea came up to use the volume of the substrate to gather charges [5]. In this paper we present a novel vertically pinned photodiode integration scheme with in-depth charge storage and enhanced full-well capacity. The studied pixel architecture seems particularly suitable for back illuminated small size pixels.

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II. VERTICALLY PINNED PHOTODIODE

A. Pixel Architecture

The pixel we chose to investigate in this paper is a 1.4 µm pitch, back illuminated, 2 transistors (2T) architecture with embedded N-type, vertically pinned photodiode. A simplified layout of the pixel is depicted in figure 1. Compared to traditional pixel architectures, the photodiode used to collect the photo-generated charges has its two pinning junction layers perpendicular to the silicon surface. A cross-sectional simulation of the realized photodiode is presented in figure 2. The pixel is optimized to store the collected charges in the depth of the pixel (up to 1.5 µm depth). We chose deep trench isolation (DTI) technique to

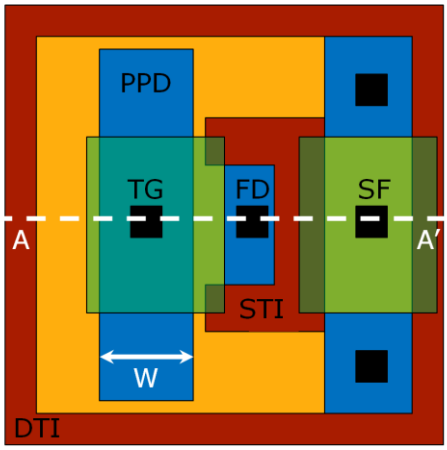

Fig. 1. Simplified pixel top view showing transfer gate (TG), pinned photodiode (PPD), floating diffusion (FD), source follower (SF), shallow trench isolation (STI), deep trench isolation (DTI). N-type doping are plotted in blue, P-type doping are plotted in orange.

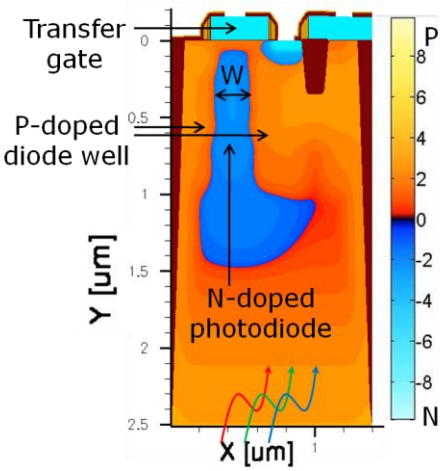

Fig. 2. Cross-sectional simulation of the vertically pinned photodiode along the AA' cross-section. N-type doped regions are represented in blue, P-type doped regions are represented in orange.

avoid cross-talk between neighboring pixels [6]. As we chose to stack the transfer gate (TG) directly above the photodiode, the pixel also exhibits a novel charge transfer behavior. This choice does not impact sensitivity since the pixel is backside illuminated. The photodiode does not need to be self-aligned with the TG any more to ensure proper transfer of the charges. The photodiode deliberately shows a pear shape with an extended region near the backside. Due to that shape, charges generated near the back surface cannot diffuse toward the drain of the MOS pixels sharing the same well as the photodiode. This specific lateral spreading must be carefully implemented since it can be source of charge lag if too heavily doped.

B. Fabrication Process

In order to fabricate a vertically pinned photodiode, we realized multiple-step high energy implantations. These implantations were performed at 0 tilt angles, so as to take benefit of channeling effects in silicon, which makes it possible to dope the substrate deeper. Such high energy implantation steps were possible because the photodiode is

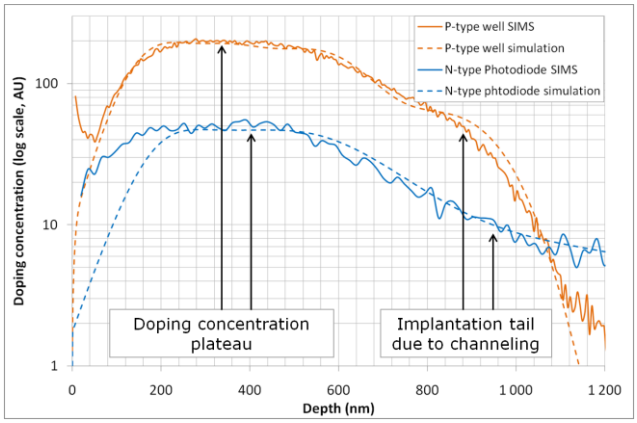

Fig. 3. Doping concentration profiles in the photodiode and in the diode well (SIMS analysis and simulation).

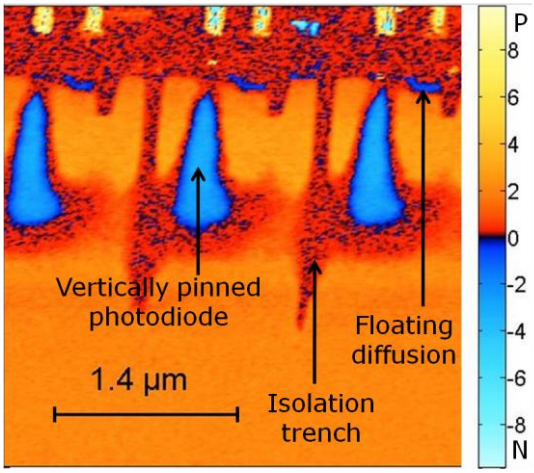

Fig. 4. SCM analysis along the AA' cross-section. N-type doped regions are represented in blue, P-type doped regions are represented in orange.

no more self-aligned to the TG.

Thanks to TCAD simulation tools we adjusted the N-type photodiode implantation doses in order to form a doping concentration plateau in the substrate. In the same manner, the implantation doses of the photodiode's P-type well were settled so that the junctions of the photodiode stay equidistant over the entire depth of the photodiode to ensure constant photodiode depletion potential (maximum of electrostatic potential present in the depleted photodiode region) in the entire depth. Doing so, it is possible to guarantee an in depth storage of the photo-generated charges by maximizing the full well capacity of the photodiode. Figure 3 shows the secondary ions mass spectrometry (SIMS) analysis of both the photodiode and the well doping concentration (real and simulated). The curves show a doping concentration plateau and an implantation tail, due to channeling effect.

Additional thermal treatments can be used to let the impurities of the wells diffuse and so narrow the width of the photodiode. As we will see in the next section the diode potential is directly linked to diode width. Figure 4 illustrates a scanning capacitance microscopy (SCM) along the AA' cross-section and should thus be compared to figure 2, both show good matching.

In order to further increase the quantum efficiency (QE), we have chosen a built-in ONO antireflective layer, realized by a specific SOI wafer process. After the deposition of a triple layer, composed of oxide, nitride and oxide on a silicon bulk wafer, hydrogen is implanted through the dielectric stack. Afterwards the so prepared substrate is bonded to another wafer by means of molecular oxide-oxide wafer bonding. After a thermal annealing the final substrate is obtained. The initial SOI layer (around 100nm) is reinforced to a thickness of several micrometers by epitaxial growth in order to increase light absorption. Figure 5 depicts the successive process steps needed in order to form this ONO ARC. Special care has to be taken in order to avoid charge accumulation in the nitride layer [7] which might

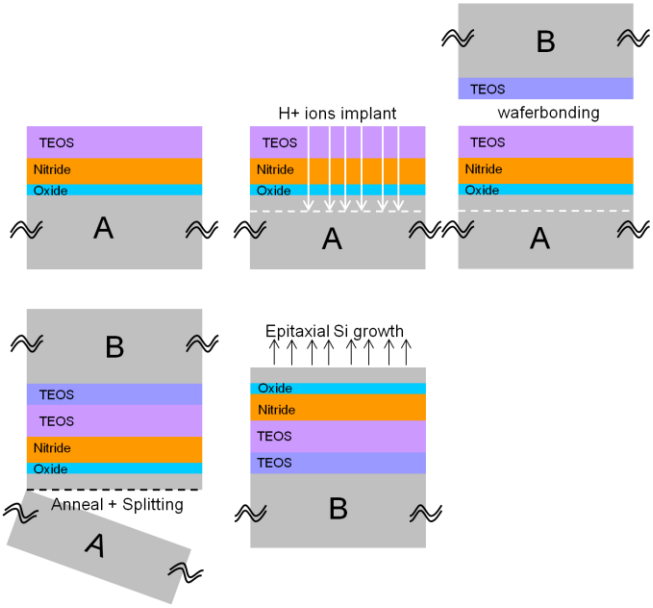

Fig. 5. Successive steps in forming the built-in ONO broadband antireflective coating using Smart Cut™ technology.

lead to performance loss. A special low damage process has been developed in order to avoid this charge accumulation.

C. Photodiode depletion potential

As already mentioned, it is possible to control the diode depletion potential by modifying the width of the photodiode. This width can be modulated by design, by implantation doses utilized to form the photodiode or by adding a thermal treatment after diode implantation. We performed diode depletion potential measurements on dedicated test structures. Figure 6 shows the effect of doping and additional thermal treatment on diode depletion potential. Plotting the diode depletion potential versus diode width (W), one sees that the diode depletion potential follows a quadratic law. When solving Poisson's equation along the pinning dimension for abrupt junctions at thermal equilibrium in an entirely depleted photodiode, we find following expression for the diode depletion potential:

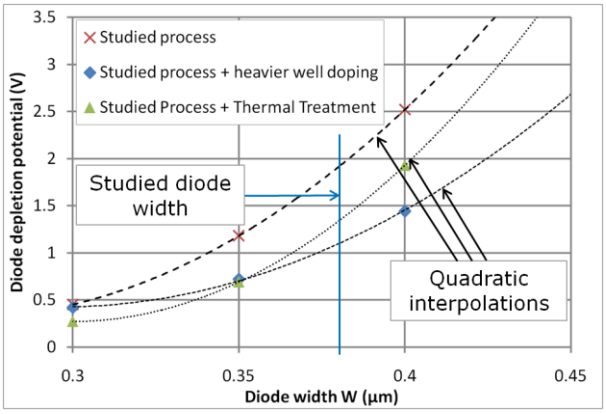

Fig. 6. Diode potential vs diode width for 3 types of processes. Additional quadratic interpolation curves have been added.

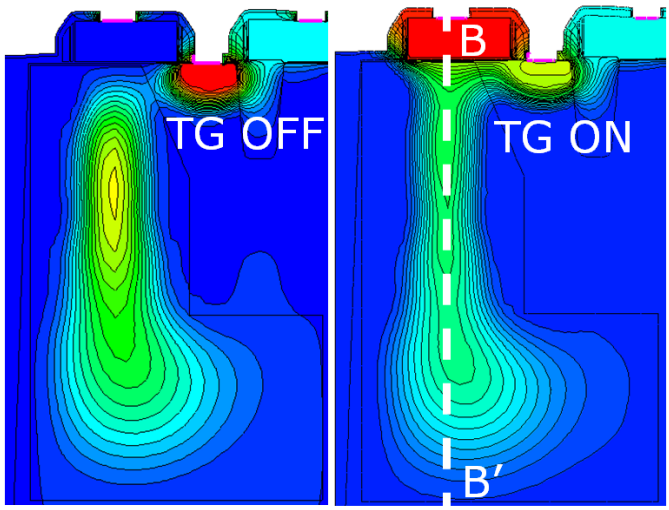

Fig. 7. Electrostatic potential along the AA' cross-section, when TG is turned ON and OFF in a depleted photodiode.

$$\psi_{DDP} = \frac{e \cdot N_d \cdot W^2}{2 \cdot \varepsilon_{Si}} + \psi_B \qquad (1)$$

Where ψ_{DDP} is the diode depletion potential, e is the electronic charge, N_d is the doping concentration of the photodiode, W is the width of the photodiode as represented in figure 1, ε_{Si} is the absolute permittivity in silicon and ψ_B is the bulk potential.

Since the measured potential follows a quadratic law according to W we can assert that the photodiode is laterally pinned. As we can see in figure 6, increasing the photodiode well doping concentration or adding a thermal treatment narrows the diode width and so decreases its potential. These effects are in accordance with equation (1).

D. Charge Transfer

Our pixel exhibits a unique charge transfer method, since the TG is directly located above the photodiode. Doing so, the role of the TG is to bring the charges stored in the bulk in its surface channel where they are then transferred to the

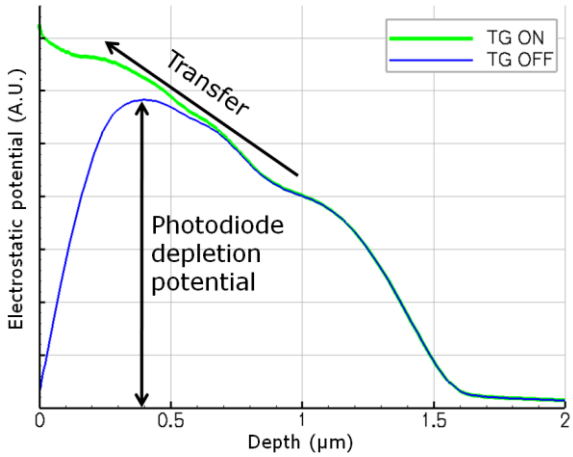

Fig. 8. Electrostatic potential profile along the BB' cross-section, when TG is turned ON and OFF in a depleted photodiode.

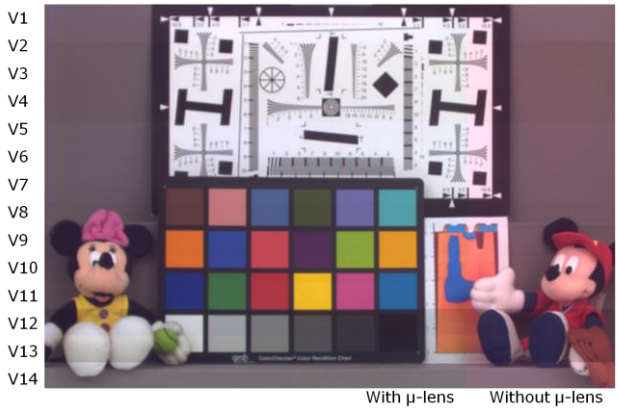

Fig. 9. Picture taken with a multiple pixel array at 500 lux ambient light at 3200K light temperature and F number 2.8.

floating diffusion. Figure 7 depicts the electrostatic potential in the pixel along the AA' cross-section when the TG is turned ON and OFF and the photodiode is empty of charges. Figure 8 shows the electrostatic potential profile along the BB' cross-section. We can see that when the TG is turned ON, it lowers the surface potential sufficiently to let the charges flow toward the surface. The potential in the depth of the photodiode remains the same since it is pinned laterally.

III. ELECTRO-OPTICAL MEASUREMENTS

The measurements results given hereafter were realized on a pixel array comprising multiple pixel versions. Table 1 gives a summary of the best pixel's performances.

The studied pixel has a full well capacity of 11000 electrons. Contrary to planar diode architecture, full-well capacity does not vary quadratically with pixel size but linearly. Thus, thanks to vertically pinned diode architecture, full-well capacities of 8700 electrons could be expected for 1.1µm pixel pitch size. Also the implantation depth can be increased by adding implantation steps with even higher implantation energies and thus higher full well capacities can be achieved.

Figure 9 is a picture taken with a multiple pixel array. It has been taken at 15 frames per second (66 ms), for an ambient light of 500 lux at 3200K light temperature, with an objective of focal length 12 mm and F number 2.8.

The improvements brought by the specific ONO broadband ARC can be seen in figure 10, representing the

TABLE I
PIXEL PERFORMANCES

Quantity	Units	Value
Conversion Factor	µV/e-	145
Full-well capacity	e-	11000
Dark current (at 60°C)	e-/s	50
Charge lag		< 0.2% of full well capacity

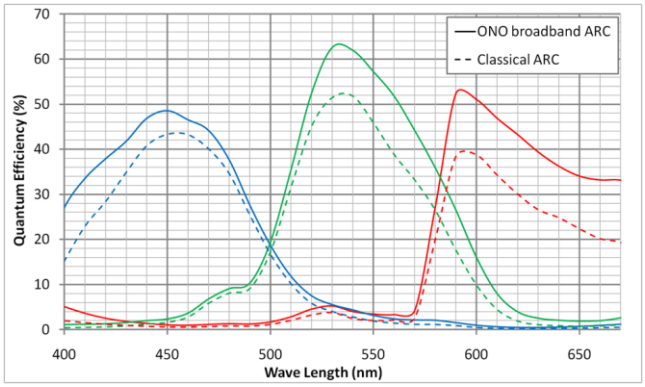

Fig. 10. Quantum efficiency for classical ARC and optimized ONO broadband ARC.

QE curves of both, classical ARC and ONO broadband ARC. An improvement of QE is observable in the three color channels with more than 10% in the green and red spectrum.

IV. CONCLUSION

We have realized a vertically pinned photodiode with a 1.4 µm pitch. Thanks to diode architecture with TG stacked above the vertically pinned photodiode and due to an optimized doping profile, we achieved a high full-well capacity of 11000 electrons and a low charge lag. The application of a broadband ARC resulted in a QE of 63% in the green spectrum.

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